

1 **ABSTRACT**

2 A memory controller prevents CPUs and other I/O bus masters from  
3 accessing memory during a code (for example, trusted core) initialization process.  
4 The memory controller resets CPUs in the computer and allows a CPU to begin  
5 accessing memory at a particular location (identified to the CPU by the memory  
6 controller). Once an initialization process has been executed by that CPU, the  
7 code is operational and any other CPUs are allowed to access memory (after being  
8 reset), as are any other bus masters (subject to any controls imposed by the  
9 initiated code).

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